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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,079	03/28/2001	Grant Kloster	42390P11026	4031

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EXAMINER	
MAGEE, THOMAS J	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/820,079	KLOSTER ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10 and 12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10, and 12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 5 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 6,211,061 B1) in view of Fink et al. ("Standard Handbook for Electrical Engr." McGraw-Hill, New York (1968)) and Chao et al. (US 6,429,119 B1).

3. Regarding Claim 1, Chen et al. disclose (Col. 5, line 65 through Col. 6, line 22) a structure on a substrate comprising a diffusion barrier layer (24) (Figures 4 and 6B) having a first dielectric constant (7.5, silicon nitride), and a thickness in the range, 300 to 500 Angstroms, with a layer (30) used as a layer used as an etch stop layer (See Figure 4) above and on the diffusion barrier layer with a second thickness and a dielectric constant < 3.0 and an interlayer dielectric (34) of thickness, 3000 Angstroms, with a dielectric constant of 3.9 (silicon dioxide). Chen et al. do not disclose that the thickness of the etch stop layer (30) is less than about 600 Angstroms. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to perform a series of experiments to obtain a thin etch stop layer with optimal thickness less than 600 Angstroms to reduce parasitic capacitance (Chao et al., Col. 1, lines 6 – 11). It has been ruled by the court that "where the general

conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller,* 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Additionally, Chen et al. do not disclose the effective dielectric constant of the structure. However, the determination of effective dielectric constant is calculable from extremely simple equations notoriously well known to those of average skill in the art using elementary Physics and Electrical Engineering texts and handbooks (See for example, "Standard Handbook for Electrical Engr."). Capacitance for capacitors in series (stack of dielectric layers) is: 1/C(total) = 1/C(1) + 1/C(2) + ... And in general, C = kA/d, where k is the dielectric constant, A is area, and d is thickness. The effective dielectric constant is then approximated by: d(total)/ [(d1/k1) + (d2/k2) + (d3/k3)], where d1,k1..... refer to layer 1, etc. Substituting values disclosed by Chen et al. in the equation, the effective dielectric constant is less than three, and is therefore, an inherent property of the structure.

4. Regarding Claims 5 and 6, Chen et al. disclose (Col. 6, lines 4 – 12) that the barrier layer is inorganic (silicon nitride) and the etch stop layer is organic (FLARE, SILK).

5. Regarding Claim 7, Chen et al. disclose that an electrically conductive trace is present in the substrate (Col. 5, lines 65 – 67) (20, Figure 6B) and a contact (Col. 8, lines 1 – 2) present in a recess (45) that extends through the ILD, etch stop, and barrier layers making electrical connection to the trace.

6. Regarding Claim 8, Chen et al. do not disclose a "single" damascene structure for the

contact, but do disclose a dual (or T-shaped) damascene structure. The difference between a single and a dual damascene structure involves only a change in shape and a continuous etch through the layers for the single, whereas the dual requires two etch steps. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to alter the "shape" of the contact to produce a single damascene structure. Consistent with rulings of the court, changes in size or shape of parts of an invention, in the absence of an unexpected result, involve only routine skill in the art. In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

7. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Fink et al. and Chao et al., as applied to Claims 1, and 5 – 8, and further in view of Wang et al. (US 6,291,887 B1) and Wolf ("Silicon Processing for the VLSI Era, Vol. 4 – Deep Submicron Process Technology," Lattice Press, Sunset Beach, CA (2002), p. 641) and Gabriel et al. (US 6,448,654 B1).

Chen et al. do not disclose an organic diffusion barrier layer and an inorganic etch stop layer. However, Wang et al. disclose (Col.8, lines 16 – 21, lines 44 – 46) that the first (diffusion barrier) layer (14) (Col. 5, lines 20 – 24) is a polymer (organic) and the etch stop layer (16) is nitride (inorganic) (Col. 5, lines 36 – 38).
Further, Gabriel et al. disclose (Col. 4, lines 36 – 52) that thin (500 Angstroms) dielectric layers at the surface are desireable to provide versatility in the selection of more etch resistant materials for layers. Using the calculation for effective dielectric constant discussed earlier, it is then possible to obtain an effective dielectric constant < 3, using a

choice of low k materials (See Wolf, Figure 14-2). Hence, it would be obvious to one of ordinary skill in the art at the time of the invention to combine Wang et al., Wolf, and Gabriel et al. with Chen et al., Fink et al. and Chao et al. to provide a structure containing low k layers that would avoid undercutting (Wang et al., Col. 4, lines 58 – 62) of the first dielectric layer during etching to form damascene contacts.

8. Claims 9, 10, and 16 - 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Chao et al.

9. Regarding Claims 9 and 10, Chen et al. disclose (Col. 5, line 65 through Col. 6, line 22) a conductive trace (20) in a substrate and coplanar with the upper surface, with a structure on the substrate comprising a inorganic (silicon nitride) diffusion barrier layer (24) (Figures 4 and 6B) above and on substrate and trace, having a dielectric constant (7.5) and a thickness in the range, 300 to 500 Angstroms, with an organic layer used as an etch stop layer (See Figure 4) above and on the diffusion barrier layer and a dielectric constant < 3.0 and an interlayer dielectric of thickness, 3000 Angstroms, with a dielectric constant of 3.9 (silicon dioxide). Chen et al. do not disclose that the thickness of the etch stop layer (30) is less than about 600 Angstroms. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to perform a series of experiments to obtain a thin etch stop layer with optimal thickness less than 600 Angstroms to reduce parasitic capacitance (Chao et al., Col. 1, lines 6 – 11). It has been ruled by the court that "where the general

conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller,* 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

10. Regarding Claims 16 – 18, Chen et al. disclose (Col. 5, line 65 through Col. 6, line 22) a structure on the substrate comprising an inorganic (silicon nitride) first dielectric layer (24) (Figures 4 and 6B) above and on substrate and trace, having a dielectric constant (7.5) and a thickness in the range, 300 to 500 Angstroms, with an organic (polymer) layer used as an etch stop layer (See Figure 4) above and on the diffusion barrier layer with a dielectric constant < 3.0 and an interlayer dielectric of thickness of 3000 Angstroms, with a dielectric constant of 3.9 (silicon dioxide), wherein, a conductive damascene "plug" is present (Col. 8, lines 1 and 2) in recess 45 (Figure 6B), where the conductive layer is in contact with first dielectric layer, etch stop layer, and ILD layer.

Chen et al. do not disclose that the thickness of the etch stop layer (30) is less than about 600 Angstroms. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to perform a series of experiments to obtain a thin etch stop layer with optimal thickness less than 600 Angstroms to reduce parasitic capacitance (Chao et al., Col. 1, lines 6 – 11). It has been ruled by the court that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller,* 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

11. Claims 12 – 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Chao et al., as applied to Claims 9, 10, and 16 - 18 above, and further in view of Fink et al. and Wolf.

Chen et al. do not disclose effective dielectric constants for the ILD, etch stop, and diffusion barrier layer "stacks". As discussed for Claim 1, the effective dielectric constant is approximated (Fink et al.) by the equation: d(total)/ [(d1/k1) + (d2/k2) + (d3/k3)] , where d1,k1, ... refer to thickness and dielectric constant of layer1, etc. Using the values of thickness over the range disclosed by Chen et al. and dielectric constants of low k materials (Wolf), the approximate range of effective dielectric constants is calculated from 2.5 to 3.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to Fink et al. and Wolf with Chen et al. to obtain low effective k values for the "stack" combination.

12. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Chao et al., as applied to Claims 9, 10, and 16 –18 above, and further in view of Wolf.

Chen et al. do not explicitly disclose a dielectric constant for the etch stop layer. Wolf (Figure 14-2) discloses that SILK (one of the materials disclosed by Chen et al.) has a dielectric constant less than about 2.8. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Chen et al. and Wolf to obtain low effective k values for the "stack" combination.

13. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Chao et al., as applied to Claims 9, 10, and 16 – 18 above, and further in view of Bains ("Nanostructured Dielectrics Good Candidates for Next Generation Computer Chips," OE Reports, No. 194, (February, 2000) pp. 1 – 3).

Chen et al. do not explicitly disclose that the etch stop layer has a dielectric constant of about 2. However, Bains discloses that IBM produces a porous organosilicate dielectric material of dielectric constant equal to 2.2. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize an organosilicate material with pores to attain a low k etch stop layer for use in forming damascene interconnects, and hence to combine Bains and Chen et al.

Response to Arguments

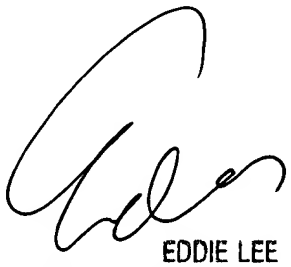
14. Applicant's arguments with respect to claims have been considered but these have been found to be unpersuasive. In particular, Applicant contends throughout the Response, based on the amendment submitted, that the limitation of an *"etch stop layer comprising a thickness less than 600 Angstroms,"* would preclude use of the Chen et al. reference. Examiner does not concur. The thickness of the etch stop layer (30) is adjustable to less than 600 Angstroms through routine experimentation to obtain optimization to lower parasitic capacitance (Chao et al., Col. 1, lines 6 – 11).

The depth of the trench (35) (Figure 7) is greater than about 4000 Angstroms, as stated by Applicant. As shown in the figure, the depth is equal to the sum of thicknesses, t, of each of the layers, T = t(50) + t(34) + t(30) + t(24), wherein T = 600 + 3000 + 600 + 500 = 4200 Angstroms, consistent with the Chen et al. disclosure.

Conclusions

15. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 571-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
July 18, 2004



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